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10/684,953	10/14/2003	Joseph B. Rowlands	BP 3257.1	4823

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EXAMINER
MANOSKEY, JOSEPH D

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	**Application No.** 10/684,953	**Applicant(s)** ROWLANDS ET AL.	
	Examiner Joseph D. Manoskey	**Art Unit** 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2007*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.
  4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-20* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on *14 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  a)☐ All b)☐ Some * c)☐ None of:
    1.☐ Certified copies of the priority documents have been received.
    2.☐ Certified copies of the priority documents have been received in Application No. _____.
    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
  Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3-13, and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kitamorn et al., U.S. Patent 7,103,808, hereinafter referred to as "Kitamorn".

3. Referring to claim 1, Kitamorn teaches an apparatus for reporting errors occurring in a data process system, where the data processing system may include a plurality of processors connected via a system bus, and where the errors are determined if they are located below the host bridge, this is interpreted as a system for detecting transaction errors in a system comprising a plurality of data processing devices using a common system interconnect bus (See Fig. 1 and Col. 1, line 61 to Col. 2, line 49). Kitamorn teaches a I/O bus bridge connected to the system bus and provides an interface to an I/O bus to connect to multiple PCI bridges, this is interpreted

as a node controller operably coupled to said system interconnect bus and a plurality of interface agents communicatively coupled to said node controller (See Fig. 1 and Col. 2, lines 44-47).

Kitamorn teaches a bad status and clearing an enabled peripheral address space upon the event of the bad status. The clearing is of a register bit and Kitamorn teaches virtualizing all the hardware resources, this is interpreted as an address table comprising a plurality of predetermined virtual register addresses corresponding to predetermined transaction error conditions (See Col. 5, lines 57-60 and Col. 7, lines 47-63). Kitamorn discloses The I/O bus bridge provides an interface to the I/O bus, this is interpreted as wherein errors corresponding to transactions between said interface agents and other processing modules in said system are directed to said node controller (See Fig. 1 and Col. 2, lines 44-47). Finally Kitamorn teaches clearing the peripheral address space in the event of a bad status and reporting errors that are determined to have occurred below the host bridge, this is interpreted as wherein said node controller is operable to flag said errors using said predetermined virtual register addresses and to communicate said errors to said system interconnect bus to be available for detection (See Col. 1, lines 63-66).

4. Referring to claim 3, Kitamorn teaches a service processor with JTAG capability, this is interpreted as further comprising a system control and debug module operably connected to said system interconnect bus (See Fig. 1, and Col. 3, line 67 to Col. 4, line 3).

5. Referring to claim 4, Kitamorn discloses the apparatus having a service processor with its own local memory and with JTAG/scan bus capability, this is interpreted as further comprising a trace cache operably connected to said system control and debug module, wherein said errors are detected by said trace cache and said system control and debug module (See Fig. 1 and Col. 3, lines 67 to Col. 4, line 9).

6. Referring to claim 5, Kitamorn teaches an error log and also teach use of error registers, this is interpreted as wherein said node controller sends said transactions corresponding to said errors to predetermined register addresses corresponding to error conditions (See Col. 8, lines 1-4).

7. Referring to claim 6, Kitamorn teaches I/O errors, this is interpreted as wherein said transactions corresponding to said errors comprise input/output transactions (See Col. 1, lines 27-31).

8. Referring to claim 7, Kitamorn teaches looking at the failing address and command, this is interpreted as wherein said transactions corresponding to said errors comprise control commands (See Col. 7, lines 64-65).

9. Referring to claim 8 and 9, Kitamorn discloses I/O errors, this interpreted as wherein said transactions corresponding to said errors comprise a writes to memory addresses and reads from memory addresses (See Col. 1, lines 27-31).

10. Referring to claim 10, Kitamorn discloses the apparatus having a service processor with its own local memory and with JTAG/scan bus capability, this is interpreted as wherein said errors communicated to said system interconnect bus are stored in said trace cache (See Fig. 1 and Col. 3, lines 67 to Col. 4, line 9).

11. Referring to claim 11, Kitamorn teaches determining if the error is I/O related, this is interpreted as wherein said trace cache is programmable to store only a predetermined set of errors corresponding to a specified diagnostic protocol (See Col. 7, lines 12-27).

12. Referring to claim 12, Kitamorn teaches a method for reporting errors occurring in a data process system, where the data processing system may include a plurality of processors connected via a system bus, and where the errors are determined if they are located below the host bridge, this is interpreted as a method for detecting transaction errors in a system comprising a plurality of data processing devices using a common system interconnect bus (See Fig. 1 and Col. 1, line 61 to Col.

Kitamorn discloses an I/O bus bridge provides an interface to the I/O bus (See Fig. 1 and Col. 2, lines 44-47). Kitamorn teaches a bad status and clearing an enabled peripheral address space upon the event of the bad status. The clearing is of a register bit and Kitamorn teaches virtualizing all the hardware resources, this is interpreted as an address table comprising a plurality of predetermined virtual register addresses corresponding to predetermined transaction error conditions (See Col. 5, lines 57-60 and Col. 7, lines 47-63). Kitamorn teaches reporting errors that are determined to have occurred below the host bridge (See Col. 1, lines 63-66). This is interpreted as detecting an error corresponding an error corresponding to a transaction between an interface agent and another processing module in said system, flagging said error using a predetermined virtual register address in an address table, said predetermined virtual register address corresponding to a predetermined transaction error condition and communicating said transaction error to said system interconnect bus for detection by a plurality of system modules coupled to said system interconnect bus.

13. Referring to claim 13, Kitamorn discloses when errors are below the host bridge, the host bridge is isolated from other portions of the data processing system, this is interpreted as said interface agent in operably connected to a switch, said switch is operable connected to a node controller, and said node controller is operably connected to said system interconnect bus (See Col. 1, line 66 to Col. 2, line 4).

14. Referring to claim 15, Kitamorn teaches an error log and also teach use of error registers, this is interpreted as wherein said node controller writes said transactions

corresponding to said errors to predetermined register addresses corresponding to error conditions (See Col. 8, lines 1-4).

15. Referring to claim 16, Kitamorn teaches I/O errors, this is interpreted as wherein said transactions corresponding to said errors comprise input/output transactions (See Col. 1, lines 27-31).

16. Referring to claim 17, Kitamorn teaches looking at the failing address and command, this is interpreted as wherein said transactions corresponding to said errors comprise control commands (See Col. 7, lines 64-65).

17. Referring to claim 18 and 19, Kitamorn discloses I/O errors, this interpreted as wherein said transactions corresponding to said errors comprise a writes to memory addresses and reads from memory addresses (See Col. 1, lines 27-31).

18. Referring to claim 20, Kitamorn discloses the apparatus having a service processor with its own local memory and with JTAG/scan bus capability, this is interpreted as wherein said errors communicated to said system interconnect bus are stored in said trace cache (See Fig. 1 and Col. 3, lines 67 to Col. 4, line 9).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 2 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Kitamorn in view of Kantake, U.S. Patent App. Pub. 2005/0080580.

21. Referring to claims 2 and 14, Kitamorn teaches all the limitations (See rejection of claims 1 and 13 respectively) except for wherein said interface agents operate in accordance with the hypertransport protocol, however Kitamorn does teach being an IBM eServer with a plurality of processors (See Col. 2, lines 30-49). Kantake discloses an IBM system with "hypertransport" (See paragraph 0015). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the system of Kitamorn with the hypertransport protocol of Kantake. This would have been obvious to one of ordinary skill in the art at the time of the invention to do because the hypertransport is a next-generation input/output interface which achieves high-rate data transfer (See Kantake, paragraph 0015).

Response to Arguments

22. Applicant's arguments filed 30 August 2007 have been fully considered but they are not persuasive. Applicant argues that Kitamorn does not teach the use of virtual

register addresses. The Examiner respectfully disagrees. Kitamorn teaches a bad status and clearing an enabled peripheral address space upon the event of the bad status. The clearing is of a register bit and Kitamorn teaches virtualizing all the hardware resources, this is interpreted as an address table comprising a plurality of predetermined virtual register addresses corresponding to predetermined transaction error conditions (See Col. 5, lines 57-60 and Col. 7, lines 47-63). This clarification has been added to the above rejections.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Manoskey whose telephone number is (571) 272-3648. The examiner can normally be reached on Mon.-Fri. (7:30am to 4pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDM
September 3, 2007

Robert W Beausoliel

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